## AMENDMENT TO THE SPECIFICATION

Please amend the paragraph at page 7, line 9 - page 7, line 19 as follows:

Accordingly, the CMOS variable gain circuit of the present invention is made to have a control signal mode that makes ~~high~~ low the control signal (Vc) when a ~~low~~ high differential input voltage [(Vi+)-(Vi-)] is applied, so that both the two transistors N101 and N103 or N102 and N104 having a cascod connection operate in the saturation region. The CMOS variable gain circuit of the present invention is made to have a control signal mode that makes ~~low~~ high the control signal (Vc) when a low differential input voltage [(Vi+)-(Vi-)] is applied, so that only the two transistors N103 and N104 to when the differential input signals are applied operate in the triode region. It is thus possible to maximize the linearity regardless of the control voltage.